REMARKS

Favorable reconsideration of this application in view of the above amendments and remarks to follow is respectfully requested.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants have amended Claim 1 to positively recite the features of the claimed invention. Specifically, applicants have amended Claim 1 to positively recite that the *collector region and the isolation regions are located within a semiconductor substrate.* Support for this amendment to Claim 1 is found throughout the specification of the instant application. See, for example, Page 6, line 27-Page 8, line 3 as well as FIG. 4. Particular reference is made to Page 6, lines 30-32 whereat it is stated that "The initial structure shown in FIG. 4 comprises substrate 50 having sub-collector 54, collector region 56 and isolation regions 52 formed therein."

Applicants have also amended Claim 1 to positively recite that the recess step provides a recessed isolation surface *below an upper surface of the collector region in the semiconductor substrate and a non-recessed surface that is substantially planar with said upper surface of the collector region in the semiconductor substrate.* Support for this amendment to Claim 1 is also found throughout the specification of the instant application. See, for example, Page 8, lines 15-18 as well as FIG. 5. Note in FIG. 5, reference numeral 75 is the recessed surface of the isolation region 52 and reference numeral 80 is the non-recessed surface of the isolation region 52. The recessed surface is below the upper surface of the substrate which is defined by the collector region 56 and the non-recessed surface 80 is substantially planar with the upper surface of the substrate that is defined by the collector region 56.

Since the above amendments to the claims do not introduce new matter into the specification of the instant application, entry thereof is respectfully requested. Applicants submit that the above amendments to Claim 1, which were made to clarify the present claimed method, were not performed previously because it was believed that the language of Claim 1, prior to this amendment, was sufficient to describe the claimed method set forth in the present application. This, however, does not appear to be the case given the Examiner's remarks made in applying the disclosure of U.S. Patent No. 5,399,511 to Taka, et al. ("Taka, et al.") against the claimed method.

Claims 1-6 and 8 stand rejected under 35 U.S.C. § 102(b) as allegedly anticipated by Taka, et al. Claims 1-6, 8 and 10 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of U.S. Patent No. 6,352,907 to Gris ("Gris") and JP 2000-269230 ("JP '230")[1]. Claim 7 stands rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Gris and U.S. Patent No. 5,633,179 to Kamins, et al. ("Kamins, et al."). Claim 9 stands rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Gris and German Patent Publication No. DE 19652423 to Heinemann, et al. ("Heinemann, et al.").

In regard to the anticipation rejection, it is axiomatic that anticipation under § 102 requires that the prior art reference disclose each and every element of the claim to which it is applied. *In re King*, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and

[1] Applicants note that in the Official Action, the Examiner has stated that Claims 1-6, 8 and 10 are rejected under 35 U.S.C. § 102(e) as anticipated by Gris and JP '230. However, from the Examiner's statements in the Office Action, it appears that the Examiner meant that the aforementioned claims are made obvious under 35 U.S.C. § 103 as unpatentable over Gris and JP '230. If not, the Examiner's own remarks regarding the deficiency in Gris is sufficient to overcome an anticipation rejection citing Gris.

the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates anticipation. *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants respectfully submit that the claimed method of present application that is recited in Claims 1-6 and 8 is not anticipated by the disclosure of Taka, et al. Specifically, Taka, et al. do not disclose a method which includes, among other processing steps, a step of providing a semiconductor substrate comprising a collector region located at an upper surface of said semiconductor substrate and isolation regions adjacent said collector region, said *collector region and said isolation regions are located within said semiconductor substrate*, as presently recited in Claim 1, step (a). Instead, Taka, et al. disclose a method in which the collector 52 is formed on, not within, a surface of the substrate 70. As such, Taka, et al. do not disclose the providing step recited in step (a) of Claim 1.

Moreover, Taka, et al. do not teach, among other processing steps, a step of recessing a portion of the isolation regions below said upper surface of said collector region in said semiconductor substrate so as to provide a recessed isolation surface below said upper surface of said collector in the semiconductor substrate and a non-recessed surface that is substantially planar with said upper surface of the collector in the semiconductor substrate, as recited in Claim 1, step (b). Applicants first observe that Taka, et al. do not teach recessing the isolation region 46 located in the substrate 70. Taka, et al. do however disclose the etching of insulating regions 50 and 49 in defining

opening F, but not the insulating region 48. Applicants observe that the etched insulating regions 49 and 50 of Taka, et al. do not have a recessed isolation surface below an upper surface of a collector in the semiconductor substrate and a non-recessed surface that is substantially planar with the upper surface of the collector in the semiconductor substrate, as recited in Claim 1, step (b). Likewise, insulating regions 46 and 48 which are not etched in providing the opening F also do not meet the claimed feature of having a recessed isolation surface below the upper surface of the collector in the semiconductor substrate and a non-recessed surface that is substantially planar with the upper surface of the collector in the semiconductor substrate, as recited in Claim 1, step (b).

The foregoing remarks clearly indicate that the applied reference does not teach *each and every* aspect of the claimed invention, as required by *King* and *Kloster Speedsteel*; therefore the claims of the present application are not anticipated by the disclosure of Taka, et al. Applicants respectfully submit that the instant § 102 rejection has been obviated and withdrawal thereof is respectfully requested.

Turning to the various obviousness rejections raised under 35 U.S.C. § 103, applicants respectfully submit that the combined disclosures of Gris and JP '230 or Kamins, et al. or Heinenmann, et al. do not render the claimed method obvious. Specifically, the applied references do not teach or suggest applicants' claimed method which includes, among other processing steps, recessing a portion of the isolation regions below the upper surface of said collector region in the semiconductor substrate so as to provide a recessed isolation surface below the upper surface of the collector in

the semiconductor substrate and a non-recessed surface that is substantially planar with the upper surface of the collector in the semiconductor substrate.

Gris discloses a recessing step in his process (See FIG. 4), but during the recessing of the isolation region 4 the collector region 3 is overetched (See Col. 3, lines 29-38). The overetching of the collector region 3 provides a structure in which the non-recessed and the recessed surface of the isolation region 4 both have surfaces that are above the surface of the collector 3 thereby Gris does not teach or suggest applicants' claimed feature of recessing a portion of the isolation regions below the upper surface of the collector region which is in the semiconductor substrate so as to provide a recessed isolation surface below the upper surface of the collector in the semiconductor substrate and a non-recessed surface that is substantially planar with the upper surface of the collector in the semiconductor substrate.

JP '230 does not obviate the deficiency noted above on Gris since the applied reference also does not teach or suggest a method that includes applicants' claimed step of recessing a portion of the isolation regions below the upper surface of the semiconductor substrate (i.e., the collector) so as to provide a recessed isolation surface below the upper surface of the semiconductor substrate and a non-recessed surface that is substantially planar with the upper surface of the semiconductor substrate. As indicated by the Examiner, JP '230 recesses a portion of isolation region 101 below the upper surface of the substrate. The applied reference, however, does not disclose that the non-recessed surface of the isolation region 101 is substantially planar with the upper surface of the substrate 200. It is again emphasized that in the claimed method, the upper surface of the substrate is defined as containing the collector. In JP '230, the

collector 13 is formed atop the recessed isolation region 101 therefore the prior art structure does not include the claimed feature of the collector being substantially planar with the non-recessed surface of the isolation region 101.

As such, the combined disclosures of Gris and JP '230 does not render the claimed method obvious.

Kamins, et al. fail to fulfill the deficiency of Gris since Kamins, et al. also fail to teach or suggest a method including the step of recessing a portion of the isolation regions below the upper surface of said collector region in the semiconductor substrate so as to provide a recessed isolation surface below the upper surface of the collector in the semiconductor substrate and a non-recessed surface that is substantially planar with the upper surface of the collector in the semiconductor substrate. Kamins, et al. disclose a method of forming a heterojunction bipolar transistor, in which a collector, SiGe base, and emitter are formed within a window provided by a patterned oxide layer atop a substrate containing a subcollector. Kamins, et al. do not disclose recessing a portion of an isolation region and then deposited a SiGe layer atop the recessed portion of the isolation region and therefore fail to teach or suggest *recessing a portion of the isolation regions below an upper surface of the collector region so as to provide a recessed isolation surface below the upper surface of the collector in the semiconductor substrate and a non-recessed surface that is substantially planar with the upper surface of the collector in the semiconductor substrate.*

Heinemann, et al. fail to fulfill the deficiency of Gris since Heinemann, et al. also fail to teach or suggest a method including the step of recessing a portion of the isolation regions below the upper surface of said collector region in the semiconductor substrate

so as to provide a recessed isolation surface below the upper surface of the collector in semiconductor substrate and a non-recessed surface that is substantially planar with the upper surface of the collector in the semiconductor substrate. Heinemann, et al. are directed to forming a SiGe heterobipolar transistor incorporating a group V element into at least the base region of the device and is far removed from applicants' claimed method. Heinemann, et al. do not disclose recessing a portion of an isolation region and then deposited a SiGe layer atop the recessed portion of the isolation region and therefore fail to teach or suggest *recessing a portion of the isolation regions below an upper surface of the collector region so as to provide a recessed isolation surface below the upper surface of the collector in the semiconductor substrate and a non-recessed surface that is substantially planar with the upper surface of the collector in the semiconductor substrate.*

The § 103 rejections also fail because there is no motivation in the applied references, which suggests modifying the disclosed methods to include the claimed features recited in Claim 1. The § 103 rejections are thus improper since the prior art *does not* suggest this dramatic modification. The law requires that a prior art reference provide some teaching, suggestion or motivation to make the modification. *In re Vaeck*, 947 F.2d 488, 493, 20 USPQ 2d 1438, 1442 (Fed. Cir. 1991). "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch,* 972 F.2d 1260, 1266, 23 USPQ 2d 1780, 1783-84 (Fed. Cir. 1992). There is no suggestion in the prior art of applicants' claimed method as recited in Claim 1. As such, the claims of the instant application are not obvious from the disclosures of Gris

and JP '230 or Kamins, et al. or Heinemann, et al. Applicants respectfully submit that the rejections under 35 U.S.C. § 103 have been obviated; and the withdrawal thereof is respectfully requested.

Thus in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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